

SSC8L48PN6

N-Channel Enhancement Mode MOSFET

> Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D
40V	±20V	0.69mΩ@10V	245A
400	<u> </u>	1mΩ@4V5	245/4

Description

This device is N-Channel enhancement MOSFET.

Uses SGT technology and design to provide excellent

RDSON with low gate charge. This device is suitable
for use in DC-DC conversion, power switch and
charging circuit.

100% UIS + ΔVDS + Rg Tested!

> Applications

- Load Switch
- PWM Application
- Power Management
- DC-DC Conversion

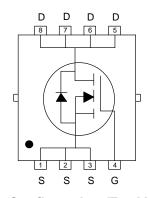
Ordering Information

Device	Package	Shipping
SSC8L48PN6	PDFN5X6-8L	5000/Reel

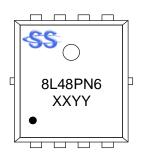
Pin configuration



PDFN5X6-8L



Pin Configuration (Top View)



Marking

(XXYY: Internal Traceability Code)



➤ Absolute Maximum Ratings (T_A=25 °C unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
V _{DSS}	Drain-to-Source Voltage		40	V
V _{GSS}	Gate-to-Source Volta	Gate-to-Source Voltage		V
1	Continuous Drain Current d	Tc=25℃	245	^
I _D	Continuous Drain Current	Tc=100℃	140	A
	Outline Davis Outline	T _A =25℃	50	
I _{DSM}	Continuous Drain Current ^a	T _A =70℃	36	A
Ідм	Pulsed Drain Curren	Pulsed Drain Current b		Α
-	Danier Biodination 6	T _C =25℃	83.3	W
P _D	Power Dissipation ^c	$T_{C}=25^{\circ}C$ $T_{C}=100^{\circ}C$ $T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$ $T_{C}=25^{\circ}C$ $T_{C}=100^{\circ}C$ $T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$ $T_{A}=70^{$	33.3	
5	Daniel Distriction 3	T _A =25℃	3.13	107
P _{DSM}	Power Dissipation ^a	T _A =70°C	2	W
las	Avalanche Current ^b L=0.5mH Single Pulse		61	Α
Eas	Avalanche Energy ^b L=0.5mH Single Pulse		930	mJ
TJ	Operation junction temperature		-55~150	°C
T _{STG}	Storage temperature range		-55~150	$^{\circ}\mathbb{C}$

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Max.	Unit
Reja	Junction-to-Ambient Thermal Resistance a	40	°C/W
$R_{ heta JC}$	Junction-to-Case Thermal Resistance	1.5	C/VV

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25°C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

SSC-V1.2 www.sscsemi.com Analog Future



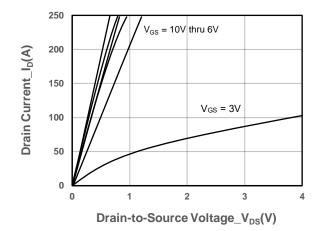


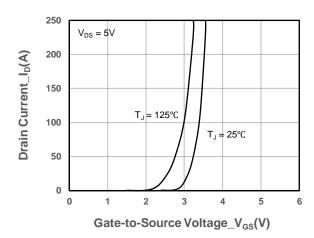
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250µA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	2	3	V
Drain-Source On-Resistance	D	V _{GS} = 10V, I _D = 30A		0.69	0.9	mΩ
Dialii-Source Oil-Resistance	$R_{DS(on)}$	V _{GS} = 4.5V, I _D = 15A		1	1.4	mΩ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Forward Voltage	V_{SD}	V _{GS} = 0V, I _S = 15A		0.78	1.4	V
Gate Resistance	R _G	V _{DS} = 0V, f = 1MHz		1.5		Ω
Input Capacitance	C _{ISS}	\\\- = 20\\ \\\- = 0\\		7450		
Output Capacitance	Coss	$V_{DS} = 20V$, $V_{GS} = 0V$, $f = 1MHz$		1340		pF
Reverse Transfer Capacitance	C _{RSS}	1 – 1101112		490		
Total Gate Charge	Q _G	V _{GS} = 10V, V _{DS} = 20V,		85		
Gate to Source Charge	Q _{GS}	$I_{D} = 20A$		25		nC
Gate to Drain Charge	Q_{GD}	1D - 20A		16		
Turn-on Delay Time	$T_{D(ON)}$			16		
Rise Time	Tr	$V_{GS} = 10V, V_{DS} = 20V,$		90		
Turn-off Delay Time	$T_{D(OFF)}$	$R_L = 2\Omega$, $R_G = 3\Omega$		150		ns
Fall Time	T _f			80		
Diode Recovery Time	Trr	I⊧=20A, di/dt=100A/us		50		ns
Diode Recovery Charge	Qrr	I⊧=20A, di/dt=100A/us		80		nC



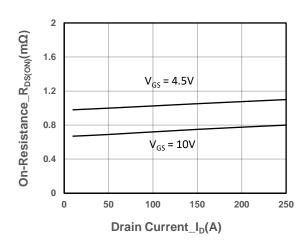
➤ Typical Performance Characteristics (T_A=25°C unless otherwise noted)

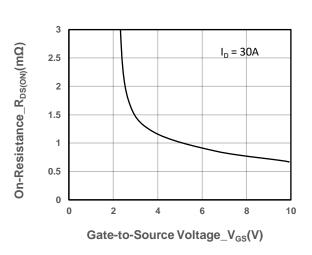




Output Characteristics

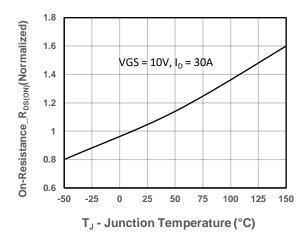


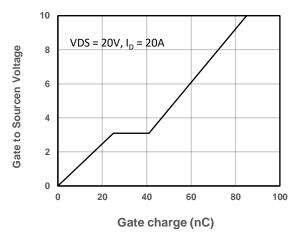




On-Resistance vs. Drain Current and Gate Voltage

On-Resistance vs. Gate-to-Source Voltage

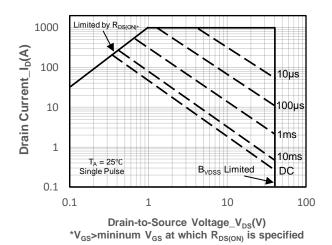




On-Resistance vs. Junction Temperature

Gate-Source Voltage vs. Gate charge

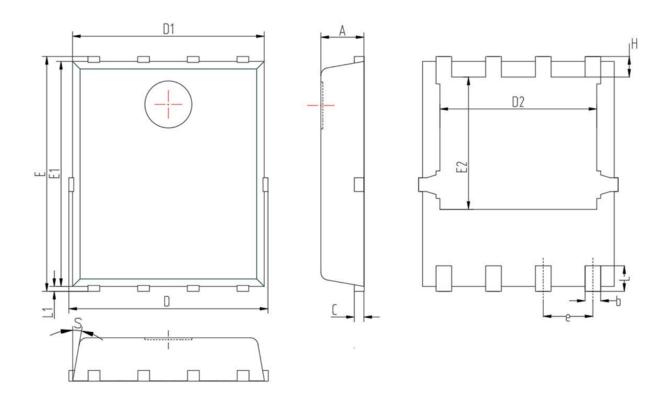




Safe Operating Area vs. Junction-to-Ambient



Package Information



Cumbal	MILL IMETER			
Symbol	Min	Nom	Max	
А	0.90	1.05	1.20	
b	0.25	0.30	0.51	
С	0.15	0.25	0.35	
D	4.80	5.10	5.40	
D1	4.80	5.00	5.20	
D2	3.70	4.00	4.30	
E	5.80	6.15	6.50	
E1	5.50	5.75	5.95	
E2	3.30	3.45	3.67	
е	1.27BSC			
Н	0.40	0.60	0.93	
L	0.45	0.65	0.85	
L1	0.00	0.10	0.25	
S	0°		12°	



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